FORM PTO-1449	ATTY. DOCKET NO.	SERIAL NO.
LIST OF PATENTS AND OTHER ITEMS FOR APPLICANTS INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	262/043	
	APPLICANT: Laurence H. Cooke, et al.	
	FILING DATE: March 19, 2001	GROUP: Not yet assigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	AA	4,858,175	8/1989	Sato	364	490	
	AB	5,519,633	5/1996	Chang et al.	364	491	
	AC	5,663,076	9/1997	Rostoker et al.	438	14	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

	AD	Merrill Hunt and Jim Rowson, "Blocking in a system on a chip," IEEE Spectrum, November 1996, pp. 35-41.
SEE COMMENT	AE	Michael Keating and Pierre Bricaud, "Reuse Methodology Manual for System-On-A-Chip Designs," Kluwer Academic Publishers, 1998.
SEE COMMENT	AF	Virtual Socket Interface Alliance Architecture Document, Version 1.0, March 1997
SEE COMMENT	AG	Virtual Socket Interface Alliance Analog/Mixed-Signal Development Working Group, "Analog/Mixed-Signal VSI Extension Specification," AMS 1 1.0, 1998
SEE COMMENT	AH	Virtual Socket Interface Alliance On-Chip Bus Development Working Group, "On-Chip Bus Attributes Specification, Version 1.0" 1998 authors.
SEE COMMENT	AI	Virtual Socket Interface Alliance Implementation/Verification Development Working Group Specification 1, Version 1.0 (1/V1 1.0), "Structural Netlist and Hard VC Physical Data Types," 1998
SEE COMMENT	AJ	"National Technology Roadmap for Semiconductors," 1997 more authors?
SEE COMMENT	AK	Steve Glaser, "IP fuels a transformation of culture, companies and cooperation," Electronic Design, January 12, 1998, pp. 55-62
SEE COMMENT	AL	"Digital Systems Testing and Testable Design," revised By Miron Abramovici, Melvin A. Breuer, and Arthur Friedman, IEEE Press Marketing, 09/1994
SEE COMMENT	AM	A J Van de Goor, "Testing Semiconductor Memories: Theory and Practice," Delft Univ. of Technology, The Netherlands, published by John Wiley, 1991
	AN	Madachy, "Knowledge-Based Risk Assessment and Cost Estimation," IEEE, pp. 172-178
	AO	Larson, et al., "Managing Design Process: A Risk Assessment Approach," IEEE Trans. on Systems, Man and Cybernetico, vol. 26, no. 6, pp. 749-759
	AP	Jacome, et al., "NREC: Risk Assessment and Planning of Complex Designs," IEEE Design & Test of Computers, pp. 42-49

COMMENT: 3 REFERENCES WERE MISSING FROM THE PARENT CASE AND CANNOT BE CONSIDERED BY THE CURRENT EXAMINER. THEREFORE, REFERENCES WILL BE CONSIDERED UPON RECEIPT OF DUPLICATES APPLICANTS AGREED TO SEND.

EXAMINER:	DATE CONSIDERED: 20-June-2002

EXAMINER: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant